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MITS

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

(Deemed to be University under section 3 of UGC Act, 1956)

EXAMINATION SECTION

ACADEMIC YEAR: 2025-26

Time Table - M.Tech. I Year I Semester (R25) Regular End Semester Examinations January 2026

TIMINGS: FN: 10:00 A.M to 01:00 PM

Date/Day	Session	Computer Science and Engineering (CSE)	VLSI Design and Embedded Systems (VES)
27.01.2026 (Tuesday)	**FN**	Advanced Data Structures and Algorithms-25MBCSETC01	CMOS Digital IC Design- 25MBVESTC01
29.01.2026 (Thursday)	**FN**	Modern Database Management Systems-25MBCSETC02	Advanced Microcontrollers and Signal Processors-25MBVESTC02
31.01.2026 (Saturday)	**FN**	Research Methodology and IPR-25MBCOMTC01	
02.02.2026 (Monday)	**FN**	Natural Language Processing- 25MBCSEDC01	FPGA Architectures and Applications-25MBVESDC03
04.02.2026 (Wednesday)	**FN**	Big Data Analytics- 25MBCSEDC04	Low Power VLSI Design-25MBVESDC04

Dated: 12.01.2026

Controller of Examinations (I/c)

CONTROLLER OF EXAMINATIONS
Madanapalle Institute of Technology & Science
(Deemed to be University)
MADANAPALLE - 517 325, A. P.

To be read in all the M. Tech-(CSE, VES) I Year I Semester Classrooms

Copy to The File Notice Board HoD-CSE HoD-ECE Transport Incharge

Note: HoD is requested to circulate among the faculty members concerned